WHAT IS CLAIMED IS:

1. A current mirror circuit comprising:

a first MOS transistor having a gate and a drain connected to the gate;

a second MOS transistor having the same channel type as the first MOS transistor, wherein the gate of the first MOS transistor is connected to a gate of the second MOS transistor; and

a compensation circuit that generates current to compensate for a decrease of mirror current that occurs according to a decline in the absolute value of the drain voltage of the second MOS transistor.

2. A current mirror circuit comprising:

a first MOS transistor having a gate and a drain connected to the gate ;

a second MOS transistor having the same channel type as the first MOS transistor, wherein the gate of the first MOS transistor is connected to the gate of the second MOS transistor; and

a compensation circuit that decreases a mirror current against an increase of a drain-source voltage dependence of the mirror current that occurs according to an increase of absolute value of the drain voltage of the second MOS transistor.

3. A current mirror circuit comprising:

a first NMOS transistor having a gate, a drain connected to the gate, and a source connected to a ground voltage;

a second NMOS transistor having a gate connected to the gate of the first NMOS transistor, and a source connected the ground voltage; and

a compensation circuit having at least one compensation NMOS transistor having a source connected to the ground voltage, and a drain connected to the drain of the second NMOS transistor;

wherein a voltage which is lower than voltage V_{g1} is applied to the gate-source voltage of the

compensation NMOS transistor, the voltage, where V_{g1} is gate-source voltage of the first and the second NMOS transistors.

4. The current mirror circuit as claimed in claim 3, wherein

the compensation NMOS transistor has a gate length and channel width, respectively equal to that of the second NMOS transistor.

5. The current mirror circuit as claimed in claim 3, wherein

voltages expressed by the arithmetic series a_k are applied to the gate-source of the at least one compensation NMOS transistor respectively,

where a_k is the arithmetic series equal to $V_{g1} - kV_{d1}$ (k=1, 2, . . ., n),

V_{d1} is the drain-source voltage of the second transistor,

V_{g1} is the gate-source voltage of the second transistor,

and n is the number of the NMOS transistors of the compensation circuit.

6. The current mirror circuit as claimed in claim 5, further comprising:

a first subtracter that generates the voltage of the first term (k=1) of the arithmetic series a_k, which is applied to the at least one NMOS transistor of the compensation circuit by the input of the voltages V_{g1} and V_{d1}; and

at least one or more subtracters that generate the voltage of second term (k=2), or after the first term (k=2,...,n) of the arithmetic series a_k by input of the voltage V_{d1} and the voltage which previous subtracter outputs.

7. The current mirror circuit according to claim 6, wherein

the input impedance of the subtracter is larger than the impedance of the operating point of the PMOS transistor or the NMOS transistor connected to the input of the subtracter.

8. The current mirror circuit according to claim 5, wherein

a subtracter generates the voltages of the arithmetic series a_k from V_{g1} and V_{d1}.

9. A current mirror circuit comprising:

a first PMOS transistor having a gate, a drain connected to the gate, and a source connected to a power source;

a second PMOS transistor having a gate connected to the gate of the first PMOS transistor, and a source connected to the power source; and

a compensation circuit having at least one compensation PMOS transistor having a source connected to the power source, and a drain connected to the drain of the second PMOS transistor;

wherein voltage which is higher than the voltage V_{g1}, which is applied to the gates of the first and the second PMOS transistors is applied to the gate-source of the compensation PMOS transistor.

10. The current mirror circuit according to claim 9, wherein

the compensation transistor has a gate length and a channel width, respectively equal to that of the second PMOS transistor.

11.The current mirror circuit according to claim 9, wherein

voltages expressed by the arithmetic series a_k are applied to the gate-source of the at least one compensation PMOS transistor respectively,

where a_k is the arithmetic series equal to $V_{g1} - kV_{d1}$ (k=1, 2, . . ., n),

V_{d1} is the drain-source voltage of the second transistor,

V_{g1} is the gate-source voltage of the second transistor,

and n is the number of the NMOS transistors of the compensation circuit.

12. A current mirror circuit comprising:

a first NMOS transistor having a gate and a drain connected to the gate, and a source connected to a ground voltage;

a second NMOS transistor having a gate connected to the gate of the first NMOS transistor, and a source connected to the ground voltage;

a PMOS transistor having a gate, a source connected to a power source, and a drain connected to the drain of the second NMOS transistor; and

a level converter that generates voltage expressed by the monotonous decrease function of the drain-source voltage that is applied to the second NMOS transistor, and applies the voltage to the gate-source of the PMOS transistor.

13. A current mirror circuit comprising:

a first PMOS transistor having a gate, a drain connected to the gate, and a source connected to a power source;

a second PMOS transistor having a gate connected to the gate of the first transistor, and a source connected to the power source;

a NMOS transistor having a drain connected to the drain of the second PMOS transistor, and a source connected to a ground voltage; and

a level converter that generates voltage expressed by the monotonous increase function of the drain-source voltage that is applied to the second NMOS transistor, and applies the voltage to the gate-source of the NMOS transistor.

14. A current mirror circuit comprising:

a first NMOS transistor having a gate, a drain connected to the gate, and a source connected to a ground voltage;

a second NMOS transistor having a gate connected to the gate of the first NMOS transistor, and a source connected to the ground voltage;

a PMOS transistor having a drain connected to the drain of the PMOS transistor, and a source connected to a power source; and

a level converter that generates voltage expressed by the monotonous increase function of the drain-source voltage that is applied to the second NMOS transistor, and applies the voltage to the gate-source of the PMOS transistor.

15. A current mirror circuit comprising:

a first PMOS transistor having a gate, a drain connected to the gate, and a source connected to a power source;

a second PMOS transistor having a gate connected to the gate of the first PMOS transistor, and a source connected to the power source;

a NMOS transistor having a drain connected to the drain of the first PMOS transistor, and a source connected to a ground voltage; and

a level converter that generates voltage expressed by the monotonous decrease function of the drain-source voltage that is applied to the second PMOS transistor, and applies the voltage to the gate-source of the NMOS transistor.

16. A current mirror circuit comprising:

a first group of at least two NMOS transistors connected in series, each of the first group of NMOS transistor has a gate, a drain connected to the gate, and a source;

a second group of NMOS transistors connected in series, the number of the second group of NMOS transistors is equal to the number of the first group of at least two NMOS transistors, each of NMOS transistor of the second group has a gate connected to the gate of corresponding to NMOS transistor of the first group, a drain, and a source; and

a third group of NMOS transistors connected to the second group of NMOS transistors, the number of the third group of NMOS transistors is equal to the number of the second group of NMOS transistors, each of the third group of NMOS transistor connects in series;

wherein the source of the last NMOS transistor of the first group of NMOS transistors, the second group of NMOS transistors, and the third group of NMOS transistors are each connected to a ground voltage, the drain of the last NMOS transistor of the second and third groups of NMOS transistors are mutually connected, difference voltages between gate-source voltages and drain-source voltages of the each second group of NMOS transistors are applied to the gate-source of the third NMOS transistors which are the same position in series as the second group of NMOS transistors respectively.

17. A current mirror circuit comprising:

a first group of at least two PMOS transistors connected in series, each of the first group of

PMOS transistor has a gate, a drain connected to the gate, and a source;

a second group of PMOS transistors connected in series, the number of the second group of PMOS transistors is equal to the number of the first group of at least two PMOS transistors, each of PMOS transistor of the second group has a gate connected to the gate of corresponding to PMOS transistor of the first group, a drain, and a source; and

a third group of PMOS transistors connected to the second group of NMOS transistors, the number of the third group of PMOS transistors is equal to the number of the second group of PMOS transistors, each of the third group of PMOS transistor connects in series,

wherein the source of the last PMOS transistor of the first group of PMOS transistors, the second group of PMOS transistors, and the third group of PMOS transistors are each connected to a power source, the drain of the last PMOS transistor of the second and third groups of PMOS transistors are mutually connected, difference voltages between gate-source voltages and each drain-source voltage of the each second group of PMOS transistors are applied to the gate source of the third PMOS transistors same position in series as the second group of PMOS transistors respectively.

18. A power source circuit comprising:

a first NMOS transistor having a source connected to a ground voltage; and

at least one or more compensation NMOS transistors;

wherein the respective drains of the compensation NMOS transistors are each connected to the drain of the first NMOS transistor,

the sources of the compensation NMOS transistors are connected to the ground voltage, and

voltages expressed by arithmetic series of a_k are applied to the gate-source voltage of each compensation NMOS transistor,

where a_k is the arithmetic series equal to $V_{g1} - kV_{d1}$ $(k=1, 2, \ldots, n)$,

V_{d1} is the drain-source voltage of the first transistor,

V_{g1} is the gate-source voltage of the first transistor,

and n is the number of the NMOS transistors of the compensation circuit.

19. A power source circuit comprising:

a first PMOS transistor having a source connected to a power-supply voltage; and

at least one or more compensation PMOS transistors;

wherein the respective drains of the compensation PMOS transistors are each connected to the drain of the first PMOS transistor,

the source of the compensation PMOS transistor is connected to the power supply voltage, and

voltages expressed by arithmetic series a_k are applied to the gate-source voltage of each compensation PMOS transistor,

where the a_k is the arithmetic series equal to $V_{g1} - kV_{d1}$ (k=1, 2, . . ., n),

V_{d1} is the drain-source voltage of the first transistor,

V_{g1} is the gate-source voltage of the first transistor,

and n is the number of the PMOS transistors of the compensation circuit.

20. A power source circuit comprising:

a first NMOS transistor group having at least two or more NMOS transistors connected in series; and

a second NMOS transistor group having at least two or more NMOS transistors connected in series;

wherein the source of the last NMOS transistor of the first NMOS transistor group and the second NMOS transistor group are each connected to a ground voltage, where the source of last NMOS transistor of a group of NMOS transistors is defined as the source terminal closest to a ground voltage,

the drain of the last NMOS transistor of the first NMOS transistor group and the second NMOS transistor group are each mutually connected, where the drain of the last NMOS

transistor of a group of NMOS transistors is defined as the drain terminal furthest from a ground voltage, and

difference voltages between gate-source voltages and drain-source voltage of the each first group of NMOS transistor are applied to the gate source of the second NMOS transistors which is in same position in series as the first group of NMOS transistors.

21. A power source circuit comprising:

a first PMOS transistor group having at least two or more PMOS transistors connected in series; and

a second NMOS transistor group having at least two or PMOS transistors connected in series;

wherein the source of the last PMOS transistor of the first PMOS transistor group and the second PMOS transistor group are each connected to a ground voltage, where the source of last PMOS transistor of a group of PMOS transistors is defined as the source terminal closest to a power source,

the drain of the last PMOS transistor of the first PMOS transistor group and the second PMOS transistor group are each mutually connected, where the last drain terminal of a group of PMOS transistors is defined as the drain terminal furthest from a power source, and

difference voltages between gate-source voltages and drain-source voltage of the each first group of PMOS transistor are applied to the gate source of the second PMOS transistors which is in same position in series as the first group of PMOS transistors.